AMENDMENTS TO THE SPECIFICATION

Applicants respectfully present the following replacement paragraph and replacement Abstract for consideration.

Replacement paragraph for page 14, lines 11-24.

When the interface cable is connected, the disconnection signal 'Select' become LO level and the PLL circuit 38 is activated and the counter 44 starts counting the leading edges of the quartz clock X'tal. And after a set number, it set the output CO to LO level and sets the internal connection signal CLKSEL to LO level. At that time the PLL circuit outputs the steady high-speed second clock PLL. On the other hand, when the interface is disconnected, the disconnection signal 'Select' becomes HI level, the PLL circuit is deactivated and stops the generation of the second clock PLL. Also, the counter 44 is preset by way of a NOR gate 46, and the output CO, as well as the internal disconnection signal CLKSEL, become HI level.

Replacement paragraph for the Abstract

One aspect of the present invention is a clock switching circuit for switching between asynchronous first clock and second clock when connecting or disconnecting an interface cable having a hot-plug function. The clock switching circuit includes a first group of flip-flops for receiving an interface disconnection signal that corresponds to disconnection and connection of the interface cable in response to the first clock, and a second group of flip-flops for receiving the interface disconnection signal in response to the second clock.